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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/670,870	09/27/2000	BOAZ OR SHRAGA	CM00914S	6829

22917 7590 04/11/2005

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EXAMINER	
SWERDLOW, DANIEL	
ART UNIT	**PAPER NUMBER**
2644	

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/670,870	SHRAGA ET AL.	
	Examiner	Art Unit	
	Daniel Swerdlow	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-37 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 24 is/are allowed.

6)☒ Claim(s) 1-3,6,7,12,15-23,25-32 and 35-37 is/are rejected.

7)☒ Claim(s) 4,5,8-11,13,14,19,33 and 34 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/11/02.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claim 19 is objected to because of the following informalities: Claim 19 recites the limitation "a digital-to-analog converter, connected to said signal processor, to said subtractor and to a source of said input signal" in line 12. The written description and Fig. 2 disclose an analog-to-digital converter so disposed. In addition, Claim 20, which depends from Claim 19, requires an analog-to-digital converter for antecedent basis. Further, in applicant's foreign priority document, the corresponding claim refers to the reference character for the analog-to-digital converter in conjunction with the recitation of "a digital-to-analog converter". As such, examiner concludes that the recitation is intended as "an analog-to-digital converter, connected to said signal processor, to said subtractor and to a source of said input signal" and is so treated in the prior art rejections made below. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 18 and 35 through 37 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. Claim 18 recites the limitation "said updated echo replica signal" in line 8. There is insufficient antecedent basis for this limitation in the claim. To advance prosecution to maximum extent possible, examiner makes prior art rejections below based on the interpretation that Claim 18 is intended to depend from Claim 17, which provides the antecedent basis.

6. Claim 35 recites the limitations "said at least two error signal amplitude measure values" in lines 6-7 and "said at least two far-end signal amplitude measure values" in lines 8-9. There is insufficient antecedent basis for this limitation in the claim. Antecedent basis for the first recitation is in Claim 33, while antecedent basis for the second recitation is in Claim 34. As such, there is no single claim dependence from which would render Claim 35 definite. As such, examiner can make no reasonable interpretation of the claim against which to apply prior art. Examiner notes that Claims 33 and 34 are both allowable matter and the incorporation of the limitations of both those claims in Claim 35 would render Claim 35 and the claims depending therefrom both definite and allowable matter.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1 through 3, 6, 7, 12 and 15 through 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Capman et al. (EP 0 854 626 A1).

9. The cited European Patent Application is prior art under 35 U.S.C. 102(b) due to its publication date of 22 July 1998. For convenience, US Patent 6,108,413 is relied upon as an English translation thereof. References are made below to text and figures as they appear in the US Patent.

10. Regarding Claim 1, Capman discloses an echo canceller (Figs. 1, 6; column 7, lines 40-53) that: delivers (i.e., determines) an echo prediction signal y(n) that corresponds to the echo-replica signal claimed and inherently has a Euclidean norm (column 1, lines 30-32); produces (i.e., determines) an observation z(n) that corresponds to the input signal claimed and inherently has a Euclidean norm (column 1, lines 27-29); calculates (i.e., determines) a gradient (i.e., gradient step size) (column 2, lines 18-32); dynamically adjusting (i.e., correcting) the coefficients of an adaptive filter (column 1, lines 38-46) to derive an updates echo-replica signal; and delivering (i.e., determining) an updated error signal by deducting (i.e., subtracting) the echo prediction (i.e., echo-replica) signal from the observation (i.e., input) signal (column 1, lines 35-37).

11. Regarding Claim 2, Capman further discloses the echo prediction (i.e., echo-replica) signal being delivered (i.e., produced) by a digital filter from the reception (i.e., reference far-end) signal x(n) (column 1, lines 30-32). Capman further discloses the filter being adaptive (column 1, lines 38-46).

12. Regarding Claim 3, Capman further discloses the observation (i.e., input) signal including local speech (i.e., a near-end speech signal), echo components of the reception signal

(i.e., an echo signal) and ambient noise (i.e., a noise signal) (Fig. 1, reference P, B, EC; column 1, lines 24-26).

13. Regarding Claim 6, Capman further discloses adaptation as a function of the reception (i.e., reference far-end) signal and the previous error signal (column 1, lines 38-46) in a gradient algorithm.

14. Regarding Claim 7, Capman discloses an echo canceller (Figs. 1, 6; column 7, lines 40-53) comprising: a filter (i.e., signal processor) (Fig. 6, reference 33; column 7, lines 46-49); an adaptation control module (Fig. 6, reference 9; column 1, lines 38-46) connected to the filter that corresponds to the signal processor claimed; an adaptive filter (Fig. 6, reference 7; column 1, lines 30-37); and a subtractor (Fig. 6, reference 8;column 1, lines 35-37) connected to the filter that corresponds to the signal processor claimed, the adaptive filter and the adaptation control module.

15. Regarding Claim 12, Capman further discloses the adaptation control module employing a gradient algorithm (i.e., determining a gradient step size) (column 1, lines 38-46).

16. Regarding Claim 15, Capman further discloses the adaptation control module dynamically adjusting (i.e., correcting) the coefficients of the adaptive filter (column 1, lines 38-46).

17. Regarding Claim 16, Capman further discloses adaptation (i.e., coefficient correction) as a function of the reception (i.e., reference far-end) signal and the previous error signal (column 1, lines 38-46) in a gradient algorithm.

18. Regarding Claim 17, Capman further discloses the adaptive filter delivering (i.e., deriving) the echo prediction (i.e., echo replica) signal from the reception signal (i.e., updated) (column 1, lines 30-32).

19. Regarding Claim 18, Capman further discloses a subtractor (Fig. 6, reference 8) deducting (i.e., subtracting) the echo prediction (i.e., echo-replica) signal from the observation (i.e., input) signal (column 1, lines 35-37) to deliver (i.e. derive) an updated error signal.

20. Regarding Claim 19, Capman further discloses an analog to digital converter (Fig. 1, reference 6) connected to the filter (Fig. 6, reference 33) that corresponds to the signal processor claimed, the subtractor (Fig. 6, reference 8) and the microphone (Fig. 1, reference 4) that corresponds to the source of the input signal claimed.

21. Regarding Claim 20, Capman further discloses the analog to digital converter (Fig. 1, reference 6) converting the output of the microphone (i.e., an analog input signal) into a digital input signal (Figs. 1 and 6, reference z(n); column 1, lines 27-29).

22. Claims 21 through 23 and 25 through 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirano (US Patent 5,608,804).

23. Regarding Claim 21, Hirano discloses an echo canceller (i.e., an echo suppression method) (Figs. 8, 15; column 12, lines 36-52) that: estimates the level (i.e., amplitude measure) of the reference input (i.e., far-end) signal (Fig. 15, reference 321; column 15, lines 46-49); estimates the level of the error signal (Fig. 15, reference 312; column 15, lines 51-54); compares a threshold based on the estimated error signal level, which itself constitutes an error signal measure estimate, with estimated level of the reference input signal producing a compared result

(i.e., a comparison value) (Fig. 15, reference 302; column 15, lines 57-61); and supplies the compared result to a noise level calculating (i.e., analyzing) circuit that produces an output signal that corresponds to the control signal claimed (Fig. 15, reference 304, 305; column 15, line 62 through column 16, line 4).

24. Regarding Claim 22, Hirano further discloses the error signal is received from an echo canceller (column 15, lines 36-46).

25. Regarding Claim 23, Hirano further discloses hardware implementation using a DSP (i.e., the far-end and error signals are digital signal blocks containing at least one digital sample) (column 8, lines 48-54).

26. Regarding Claim 25, Hirano discloses an echo canceller (i.e., an echo suppression apparatus) (Figs. 8, 15; column 12, lines 36-52) comprising: a reference input signal level estimating circuit (i.e., first amplitude estimation unit) (Fig. 15, reference 321; column 15, lines 46-49); an error signal level estimating circuit (i.e., second amplitude estimation unit) (Fig. 15, reference 312; column 15, lines 51-54); a comparator (i.e., a comparison unit) (Fig. 15, reference 302; column 15, lines 57-61) connected to the level estimating circuits; and a noise level calculating circuit (i.e., decision logic unit) connected to the comparator (Fig. 15, reference 304, 305; column 15, line 62 through column 16, line 4).

27. Regarding Claim 26, Hirano further discloses the reference input signal level estimating circuit (i.e., first amplitude estimation unit) estimates the level (i.e., amplitude measure) of the reference input (i.e., far-end) signal (Fig. 15, reference 321; column 15, lines 46-49).

28. Regarding Claim 27, Hirano further discloses the error input signal level estimating circuit (i.e., second amplitude estimation unit) estimates the level (i.e., amplitude measure) of the error signal (Fig. 15, reference 312; column 15, lines 51-54).

29. Regarding Claim 28, Hirano further discloses: the reference input signal level estimating circuit (i.e., first amplitude estimation unit) estimates the level (i.e., amplitude measure) of the reference input (i.e., far-end) signal (Fig. 15, reference 321; column 15, lines 46-49); the error input signal level estimating circuit (i.e., second amplitude estimation unit) estimates the level (i.e., amplitude measure) of the error signal (Fig. 15, reference 312; column 15, lines 51-54); and the comparator (i.e., a comparison unit) (Fig. 15, reference 302; column 15, lines 57-61) compares a threshold based on the estimated error signal level, which itself constitutes an error signal measure estimate, with estimated level of the reference input signal producing a compared result (i.e., a comparison value).

30. Regarding Claim 29, Hirano further discloses the comparator (i.e., comparison unit) supplies the compared result to the noise level calculating circuit (i.e., decision logic unit) that produces an output signal that corresponds to the control signal claimed (Fig. 15, reference 304, 305; column 15, line 62 through column 16, line 4).

31. Regarding Claim 30, Hirano further discloses the error signal is received from an echo canceller (column 15, lines 36-46).

32. Regarding Claim 31, Hirano further discloses: the reference input signal level estimating circuit (i.e., first amplitude estimation unit) estimates the level (i.e., amplitude measure) of the reference input (i.e., far-end) signal (Fig. 15, reference 321; column 15, lines 46-49); the error input signal level estimating circuit (i.e., second amplitude estimation unit) estimates the level

(i.e., amplitude measure) of the error signal (Fig. 15, reference 312; column 15, lines 51-54); and hardware implementation using a DSP (i.e., the far-end and error signals are digital signal blocks containing at least one digital sample) (column 8, lines 48-54).

33. Claim 32 is rejected under 35 U.S.C. 102(b) as being anticipated by Horna et al. (US Patent 4,645,883).

34. Regarding Claim 32, Horna discloses an echo canceller (i.e., echo suppression apparatus) (Fig. 2; Column 3, lines 11-32) comprising: a receive line detector (Fig. 2, reference 40; column 3, line 68 through column 4, line 2) that corresponds to the first amplitude estimation unit claimed; an error signal detector (Fig. 2, reference 80; column 6, lines 11-14) that corresponds to the first amplitude estimation unit claimed; comparators (Fig. 2, reference 42, 82; column 3, line 68 through column 4, line 17; column 6, lines 14-25) that correspond to the comparison unit claimed and are connected to the receive line detector and error signal detector; a delay (Fig. 2, reference 46; column 5, lines 19-23) that corresponds to the delay unit claimed and is connected to the comparators via an OR gate (Fig. 2, reference 44); and an OR gate (Fig. 2, reference 44; column 4, lines 17-20) that corresponds to the decision logic unit claimed and is connected to the delay.

Allowable Subject Matter

35. Claims 4, 5, 8 through 11, 13, 14, 33 and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

36. The following is a statement of reasons for the indication of allowable subject matter:

37. Regarding Claim 4, as shown above apropos of Claim 1, Capman anticipates all elements except the gradient step size being a function of the Euclidean norms. Capman discloses use of a constrained gradient algorithm to calculate gradient, but does not disclose use of the Euclidean norms of the echo replica and input signals. As such, the prior art fails to anticipate or make obvious the gradient step size being a function of the Euclidean norms of the echo replica and input signals. Therefore, Claim 4 is allowable.

38. Claim 5 is allowable due to dependence form Claim 4.

39. Regarding Claim 8, as shown above apropos of Claim 7, Capman anticipates all elements except the signal processor determining the Euclidean norm of an echo replica signal. Capman discloses a coherence calculator (Fig. 6, reference 42) that operates on an echo replica signal to control error signal filtering, but does not determine the Euclidean norm of the echo replica signal. As such, the prior art fails to anticipate or make obvious the signal processor determining the Euclidean norm of an echo replica signal. Therefore, Claim 8 is allowable.

40. Regarding Claim 9, as shown above apropos of Claim 7, Capman anticipates all elements except the signal processor determining the Euclidean norm of an input signal. Capman discloses a coherence calculator (Fig. 6, reference 42) that operates on an input signal to control error signal filtering, but does not determine the Euclidean norm of the input signal. As such, the prior art fails to anticipate or make obvious the signal processor determining the Euclidean norm of an input signal. Therefore, Claim 9 is allowable.

41. Claim 10 is allowable due to dependence form Claim 8.

42. Claim 11 is allowable due to dependence form Claim 9.

43. Regarding Claim 13, as shown above apropos of Claim 12, Capman anticipates all elements except the gradient step size being a function of the Euclidean norms. Capman discloses use of a constrained gradient algorithm to calculate gradient, but does not disclose use of the Euclidean norms of the echo replica and input signals. As such, the prior art fails to anticipate or make obvious the gradient step size being a function of the Euclidean norms of the echo replica and input signals. Therefore, Claim 13 is allowable.

44. Claim 14 is allowable due to dependence form Claim 13.

45. Regarding Claim 33, as shown above apropos of Claim 32, Horna anticipates all elements except the first amplitude estimation unit producing at least two measure values from a reference far end signal sequence of at least two signal blocks each containing at least one digital sample. While Horna discloses continuous estimation of the reference signal level, Horna discloses an analog embodiment and does not disclose at least two signal blocks each containing at least one digital sample. As such, the prior art fails to anticipate or make obvious the first amplitude estimation unit producing at least two measure values from a reference far end signal sequence of at least two signal blocks each containing at least one digital sample. Therefore, Claim 33 is allowable.

46. Regarding Claim 34, as shown above apropos of Claim 32, Horna anticipates all elements except the second amplitude estimation unit producing at least two measure values from an error signal sequence of at least two signal blocks each containing at least one digital sample. While Horna discloses continuous estimation of the error level, Horna discloses an analog embodiment and does not disclose at least two signal blocks each containing at least one digital sample. As such, the prior art fails to anticipate or make obvious the second amplitude estimation unit

producing at least two measure values from an error signal sequence of at least two signal blocks each containing at least one digital sample. Therefore, Claim 34 is allowable.

47. Claim 24 is allowed.

48. The following is an examiner's statement of reasons for allowance:

49. Claim 24 comprehends the limitations of Claim 23 and is allowable for the reasons stated above apropos of that claim.

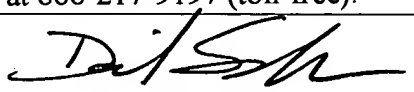
Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Swerdlow whose telephone number is 571-272-7531. The examiner can normally be reached on Monday through Friday between 7:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh H. Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel Swerdlow
Examiner
Art Unit 2644

ds
6 April 2005